## AMENDMENT TO THE CLAIMS

1. (Previously Presented) An apparatus, comprising:

a transistor having an enable terminal, an input terminal, and an output terminal, said input terminal coupled to receive binary signals that vary between first and second preselected voltage levels, and said output terminal coupled to deliver binary signals that vary between the first preselected voltage level and a third preselected voltage level;

a capacitor coupled across said input and output terminals of said transistor; and

a resistive element having a first end portion coupled to the enable terminal of said transistor and a second end portion coupled to a voltage supply to bias the transistor continuously on, the resistive element cooperating with a parasitic capacitor defined by said transistor to increase the voltage applied to the enable terminal during a transition from the first to the second preselected voltage level at the input terminal.

2. (Previously Presented) An apparatus, as set forth in claim 1, including a buffer circuit having an input terminal coupled to receive said signals that vary between the first and third preselected voltage levels.

3. (Original) An apparatus, as set forth in claim 2, wherein said buffer circuit includes an inverter.

4. (Previously Presented) An apparatus, as set forth in claim 3, including a pull-up transistor coupled between the input of said inverter and a voltage supply, and having an enable terminal coupled to the output of said inverter.

5. (Original) An apparatus, as set forth in claim 4, wherein said pull-up transistor comprises a PMOS-type transistor.

6. (Original) An apparatus, as set forth in claim 1, wherein said resistive element comprises a resistor.

7. (Original) An apparatus, as set forth in claim 1, wherein said resistive element comprises an active transistor.

8. (Currently Amended) An apparatus for converting first digital signals that vary between a first and second preselected voltage levels to second digital signals that vary between the first and a third preselected voltage level, comprising:

a pass gate transistor having a gate, source, and drain, said drain coupled to ~~to~~ receive said first signals, said source coupled to deliver said second signals, said gate coupled to a voltage supply;

a capacitor coupled across said source and drain of said pass gate transistor; and

a pump coupled to the gate of said pass gate transistor, said pump being configured to increase the voltage level applied to said gate during a transition from the first to the second preselected voltage levels.

9. (Previously Presented) An apparatus, as set forth in claim 8, wherein said pump includes a resistive element coupled between the gate of said pass gate transistor and said voltage supply, and a capacitor coupled to the gate of said pass gate transistor to receive said first digital signals.

10. (Original) An apparatus, as set forth in claim 9, wherein said capacitor coupled to the gate of said pass gate transistor is a parasitic capacitor.

11. (Original) An apparatus, as set forth in claim 9, wherein said resistive element is a resistor.

12. (Original) An apparatus, as set forth in claim 9, wherein said resistive element is an active transistor.

13. (Previously Presented) An apparatus for converting an input signal that varies between first and second preselected voltage levels to an output signal that varies between the first preselected voltage level and a third preselected voltage level, comprising:

a first circuit;

a pass gate transistor having a gate, source, and drain, said drain coupled to receive said input signal, said source coupled to deliver said output signal, said gate being coupled to a voltage supply;

a capacitor coupled across said source and drain of said pass gate transistor; and

means for increasing the voltage level applied to said gate during a transition of the input signal from the first to the second preselected voltage level.

14. (Previously Presented) An apparatus, as set forth in claim 13, wherein said means for increasing the voltage level applied to said gate for a preselected period of time.

15. (Previously Presented) A method for converting an input signal that varies from 0 volts to a first preselected voltage level to an output signal that varies from 0 volts to a second preselected voltage level, comprising:

charging a gate of a pass gate transistor to a third preselected voltage level to enable the pass gate transistor to pass at least a portion of the input signal to an output node;

charging the gate of the pass gate transistor to a fourth preselected voltage level for a preselected period of time, said fourth preselected voltage level being greater than said third preselected level; and

passing at least a portion of any AC component in said input signal to said output node.

16. (Previously Presented) A method, as set forth in claim 15, wherein charging the gate of the pass gate transistor to a fourth preselected voltage level includes charging the gate of the pass gate transistor to a fourth preselected voltage level for a preselected period of time during a transition in said input signal from 0 volts to the first preselected voltage level.

17. (Previously Presented) A buffer circuit, comprising:

a pass gate transistor having a gate, source, and drain, said drain coupled to receive a first digital signal that varies between first and second voltage levels;

a first voltage supply coupled to the gate of said pass gate transistor to bias the transistor continuously on;

a capacitor coupled across the source and drain of said pass gate transistor;

an inverter having an input terminal and an output terminal, said input terminal coupled to the source of said pass gate transistor to receive a second

digital signal that varies between the first voltage level and a third voltage level;

a pull-up transistor having a source coupled to a second voltage supply, a drain coupled to the source of said pass gate transistor, and a gate coupled to the output terminal of said inverter; and

a resistive element coupled between said first voltage supply and the gate of said pass gate transistor, the resistive element cooperating with a parasitic capacitor defined by the drain and gate of said pass gate transistor to increase the applied voltage to the gate of said pass gate transistor.

18. Canceled.

19. (Previously Presented) The buffer circuit of claim 17, wherein the resistive element comprises a resistor.

20. (Previously Presented) The buffer circuit of claim 17, wherein the resistive element comprises a PMOS-type transistor having a gate coupled to ground, a drain coupled to the gate of the pass gate transistor, and a source coupled to the first voltage supply.